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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,051	02/27/2002	Bo Soon Chang	CYPR-PM01031	8809

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EXAMINER	
BARNES, CRYSTAL J	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,051	CHANG, BO SOON	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is an initial Office Action upon examination of the above-identified application on the merits. Claims 1-29 are pending in this application.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
It does not include the inventor's signature.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: reference numbers "500" in figure 5, "650" in figure 6, "750" in figure

7, "800" in figure 8, "1000" in figure 10, "1100" in figure 11, "1200" in figure 12 and "1350" in figure 13.

5. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4 and 6-15 are rejected under 35 U.S.C. 102(e) as being anticipated by USPN 6,154,714 to Lepejian.

As per claim 1, the Lepejian reference discloses a method of performing reject management within a back-end integrated circuit (IC) device manufacturing process comprising: automatically tracking locations (see column 4 lines 29-34, "inspection stations 12, 14, 16, 18") of a die-strip ("wafer") as it traverses through said back-end manufacturing process ("defect processing system 10"); collecting parameter information (see column 4 lines 35-39, "data") regarding a plurality of die ("die") on said die-strip ("wafer"), said parameter information ("data") collected at a plurality of said locations ("inspection stations 12, 14, 16, 18") within said back-

end manufacturing process ("defect processing system 10"); using said parameter information ("data") to update a die-strip map database (see column 4 lines 35-42, "database 26") for said die-strip ("wafer") and wherein said die-strip map database ("database 26") comprises a respective entry for each die ("defects") of said die-strip ("wafer"); and automatically categorizing (see column 4 lines 39-42, "segregated") individual die ("defects") of said die-strip ("wafer") based on said die-strip map database ("database 26").

As per claim 4, the Lepejian reference discloses said collecting parameter information ("data") comprises using a tester sub-station (see column 4 lines 26-27, "test station 20") to electronically test said plurality of die (see column 3 lines 49-51, "die") of said die-strip ("wafer").

As per claim 6, the Lepejian reference discloses said parameter information ("data") comprises processing history information (see column 5 lines 64-67, "historical knowledge base") and wherein said die-strip map database ("database 26") further comprises a processing history ("all identified defects") of said die-strip ("wafer").

As per claim 7, the Lepejian reference discloses said automatically categorizing ("segregated") comprises evaluating said die-strip processing history

("historical knowledge base") to identify die-strip processing errors ("defects") which occur during said back-end manufacturing process ("defect processing system 10").

As per claim 8, the Lepejian reference discloses said automatically categorizing ("segregated") comprises assigning a category to dies of said die-strip ("wafer") and wherein said categories comprise: die acceptance (see column 9 lines 55-59, "die is acceptable"); and die rejection (see column 11 lines 6-7, "die is rejected").

As per claim 9, the Lepejian reference discloses said automatically categorizing further comprises automatically separating accepted die from rejected die (see column 3 lines 54-56, "die may be removed") into different containers.

As per claim 10, the Lepejian reference discloses said categories further comprise performance information (see columns 5-6 lines 60-9, "defect attributes file 32") of said individual die.

As per claim 11, the Lepejian reference discloses said automatically categorizing further comprises automatically separating die of different performances ("defect attributes file 32") into different containers (see column 6

lines 2-9, "the probability of a defect being conductive, the probability of the defect "evaporating" before causing a failure (i.e. subsequent processing results in the defects being removed), the variation in actual size based on the measured size, the variation in actual location based on the measured location, likely failure mechanisms and failure signatures for particular defects, and testing scenarios most likely to detect the failure mechanism of particular defects").

As per claim 12, the Lepejian reference discloses said die-strip (see column 5 lines 34-35, "silicon wafer") is of a ball grid array type (see column 5 lines 33-34, "memory arrays").

As per claim 13, the Lepejian reference discloses said back-end manufacturing process ("defect processing system 10") comprises a plurality of integrated in-line sub-stations (see column 4 lines 20-22, "in-line defect inspection stations 12, 14, 16, 18") and further comprising traversing said die-strip (see column 4 lines 29-34, "wafer") in an in-line fashion through said plurality of integrated in-line sub-stations ("inspection stations 12, 14, 16, 18").

As per claim 14, the Lepejian reference discloses a method of reject management within a back-end IC manufacturing process comprising: automatically traversing a die-strip (see column 4 lines 29-34, "wafer") through a plurality of

integrated sub-stations (see column 4 lines 20-22, "in-line defect inspection stations 12, 14, 16, 18") of said back-end manufacturing process ("defect processing system 10"), wherein said traversing is performed in an in-line fashion through said sub-stations ("in-line defect inspection stations 12, 14, 16, 18") and wherein further said die-strip ("wafer") comprises a plurality of individual die (see column 5 lines 33-35, "die"); and automatically inspecting said die-strip (""wafer) at some of said sub-stations ("in-line defect inspection stations 12, 14, 16, 18") using vision camera systems (see column 1 lines 53-57, "optical techniques"); and automatically updating a memory stored database (see column 4 lines 35-39, "database 26") with results ("data") obtained from said inspecting ("examined"), said database ("database 26") storing information for each die ("detected defects") of said die-strip ("wafer").

As per claim 15, the Lepejian reference discloses further comprising: automatically inspecting said plurality of individual die ("die") of said die-strip ("wafer") at a tester sub-station (see column 4 lines 25-26, "test station 20") of said back-end manufacturing process ("defect processing system 10"); and automatically updating said memory stored database ("database 26") with results

("data") obtained from said inspecting ("examined") of said tester sub-station ("test station 20").

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 3, 5, 16-26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,154,714 to Lepejian in view of USPN 5,943,551 to Schemmel et al.

As per claim 2, the Lepejian reference does not expressly disclose said automatically tracking comprises employing a plurality of vision camera systems deployed at said locations to automatically recognize a unique code on said die-strip which identifies said die-strip.

The Schemmel et al. reference discloses

(see column 3 lines 54-57, "Alternative positions for the wafer ID reader 24 will be apparent to those of skill in the art in light of the present disclosure. The wafer ID reader 24 identifies each unique silicon wafer 16, and transfers the information to a computer 32.")

(see column 4 lines 37-39, "The wafer ID reader 24 informs the computer 32 as to the identity of the silicon wafer 16 to be imaged for processing and storage purposes.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the optical techniques taught by the Lepejian reference to include the wafer ID reader taught by the Schemmel et al. reference to provide information identifying each silicon wafer.

One of ordinary skill in the art would have been motivated to modify the optical techniques to include the wafer ID reader so that the processing system is provided with information identifying each silicon wafer to facilitate accurate inspections of silicon dies on silicon wafers.

As per claim 3, the Lepejian reference discloses said collecting parameter information ("data") comprises using said plurality of vision camera systems ("optical techniques") to automatically analyze physical attributes (see column 1

lines 58-63, "defect density, defect size, location") of said plurality of die ("die") of said die-strip ("wafer").

As per claim 5, the Lepejian reference discloses said collecting parameter information ("data") further comprises using a tester sub-station (see column 4 lines 26-27, "test station 20") to electronically test said plurality of die (see column 3 lines 49-51, "die") of said die-strip ("wafer").

As per claim 16, the Lepejian reference does not expressly disclose further comprising: using said vision camera systems to automatically identify a code associated on said die-strip; and using said code to automatically determine a location of said die-strip within said plurality of integrated sub-stations.

The Schemmel et al. reference discloses

(see column 3 lines 54-57, "Alternative positions for the wafer ID reader 24 will be apparent to those of skill in the art in light of the present disclosure. The wafer ID reader 24 identifies each unique silicon wafer 16, and transfers the information to a computer 32.")

(see column 4 lines 37-39, "The wafer ID reader 24 informs the computer 32 as to the identity of the silicon wafer 16 to be imaged for processing and storage purposes.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the optical techniques taught by the Lepejian reference to include the wafer ID reader taught by the Schemmel et al. reference to provide information identifying each silicon wafer including its location.

One of ordinary skill in the art would have been motivated to modify the optical techniques to include the wafer ID reader so that the processing system is provided with information identifying each silicon wafer including its location to facilitate accurate inspections of silicon dies on silicon wafers.

As per claim 17, the Lepejian reference discloses said memory stored database ("database 26") maintains a processing history ("all identified defects") of said die-strip ("wafer").

As per claim 18, the Lepejian reference discloses further comprising automatically categorizing ("segregated") die ("defect") of said die-strip ("wafer") based on said information ("data") of said database ("database 26").

As per claim 19, the Lepejian reference discloses said information ("data") of said database ("database 26") comprises die category assignments for each die ("die") of said die-strip ("wafer") and wherein said die categories comprise: die acceptance (see column 9 lines 55-59, "die is acceptable"); and die rejection (see column 11 lines 6-7, "die is rejected").

As per claim 20, the Lepejian reference discloses comprising automatically sorting said plurality of die ("dies") of said die strip ("wafer") into different containers (see column 3 lines 54-56, "die may be removed") based on their category assignment ("die is acceptable/rejected").

As per claim 21, the Lepejian reference discloses a system for reject management within a back-end IC manufacturing process comprising: a plurality of integrated sub-stations (see column 4 lines 20-22, "in-line defect inspection stations 12, 14, 16, 18") performing back-end manufacturing processes ("defect processing system 10") on a die-strip strip (see column 4 lines 29-34, "wafer") traversing therethrough; a plurality of vision camera systems (see column 1 lines 53-57, "optical techniques") deployed within some of said plurality of integrated sub-stations ("in-line defect inspection stations 12, 14, 16, 18") for automatically

identifying a code associated with said die-strip ("wafer") to determine a location ("location, position") of said die-strip ("wafer") and also for automatically examining (see column 4 lines 35-39, "examined") a plurality of die (see column 5 lines 33-35, "die") on said die-strip ("wafer") for physical attributes (see column 5 lines 45-50, "wafer definition file 30") thereof; and a computer system (see column 4 lines 35-39, "data processing system 22") coupled to said vision camera systems ("optical techniques") and comprising a memory (see column 4 lines 55-58, "file 28") for integrating results ("data") of said vision camera systems ("optical techniques") for each die ("die") of said die-strip ("wafer") into a database (see column 4 lines 35-39, "database 26").

The Lepejian reference does not expressly disclose a plurality of vision camera systems for automatically identifying a code associated with said die-strip to determine a location of said die-strip.

The Schemmel et al. reference discloses

(see column 3 lines 54-57, "Alternative positions for the wafer ID reader 24 will be apparent to those of skill in the art in light of the present disclosure. The wafer ID reader 24 identifies each unique silicon wafer 16, and transfers the information to a computer 32.")

(see column 4 lines 37-39, "The wafer ID reader 24 informs the computer 32 as to the identity of the silicon wafer 16 to be imaged for processing and storage purposes.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the optical techniques taught by the Lepejian reference to include the wafer ID reader taught by the Schemmel et al. reference to provide information identifying each silicon wafer including its location.

One of ordinary skill in the art would have been motivated to modify the optical techniques to include the wafer ID reader so that the processing system is provided with information identifying each silicon wafer including its location to facilitate accurate inspections of silicon dies on silicon wafers.

As per claim 22, the Lepejian reference discloses one of said plurality of integrated sub-stations is a tester (see column 4 lines 20-22, "test station 20") for performing electronic testing (see column 4 lines 26-27, "DUT 24") of said plurality of die ("die") of said die-strip ("wafer") and wherein results (see column 4 lines 55-57, "file 28") of said tester ("test station 20") are integrated with said results (see column 5 lines 45-50, "file 30") of said vision camera systems within said database ("database 26").

As per claim 23, the Lepejian reference discloses one of said plurality of integrated sub-stations ("in-line defect inspection stations 12, 14, 16, 18") is a sorting sub-station for sorting said plurality of die ("defects") into different containers (see column 11 lines 6-7, "die is rejected") based on information ("data") stored said database ("database 26").

As per claim 24, the Lepejian reference discloses said die-strip (see column 5 lines 34-35, "silicon wafer") is of a ball grid array type (see column 5 lines 33-34, "memory arrays") and wherein said die-strip (see column 4 lines 29-34, "wafer") traverses through said plurality of integrated in-line sub-stations ("inspection stations 12, 14, 16, 18") in an in-line fashion (see column 4 line 21, "in-line").

As per claim 25, the Lepejian reference discloses said database ("database 26") contains die category assignments for each die ("defect") of said die-strip ("wafer") and wherein said die categories comprise: die acceptance (see column 9 lines 55-59, "die is acceptable"); and die rejection (see column 11 lines 6-7, "die is rejected").

As per claim 26, the Lepejian reference discloses said database ("database 26") contains a die category assignment for each die ("die") of said die-strip ("wafer") and wherein said die categories comprise: die acceptance (see column 9

lines 55-59, "die is acceptable"); die rejection (see column 11 lines 6-7, "die is rejected"); and die performance (see columns 5-6 lines 60-9, "defect attributes file 32").

As per claim 28, the Lepejian reference discloses a system for reject management within a back-end IC manufacturing process comprising: a plurality of integrated sub-stations (see column 4 lines 20-22, "in-line defect inspection stations 12, 14, 16, 18") performing back-end manufacturing processes ("defect processing system 10") on a die-strip strip (see column 4 lines 29-34, "wafer") traversing therethrough in an in-line fashion (see column 4 line 21, "in-line"); a plurality of vision camera systems (see column 1 lines 53-57, "optical techniques") deployed within some of said plurality of integrated sub-stations ("in-line defect inspection stations 12, 14, 16, 18") for automatically identifying a code associated with said die-strip ("wafer") to determine a location ("location, position") of said die-strip ("wafer") and also for automatically examining (see column 4 lines 35-39, "examined") a plurality of die (see column 5 lines 33-35, "die") on said die-strip ("wafer") for physical attributes (see column 5 lines 45-50, "wafer definition file 30") thereof; a tester sub-station (see column 4 lines 20-22, "test station 20") for

performing electronic testing (see column 4 lines 26-27, "DUT 24") of said plurality of die ("die") of said die-strip ("wafer"); and a computer system (see column 4 lines 35-39, "data processing system 22") coupled to said vision camera systems ("optical techniques") and coupled to said tester sub-station ("test station 20") and comprising a memory (see column 4 lines 55-58, "file 28") for integrating results ("data") of said vision camera systems ("optical techniques") and said tester sub-station ("test station 20") for each die ("die") of said die-strip ("wafer") into a database (see column 4 lines 35-39, "database 26").

The Lepejian reference does not expressly disclose a plurality of vision camera systems for automatically identifying a code associated with said die-strip to determine a location of said die-strip.

The Schemmel et al. reference discloses

(see column 3 lines 54-57, "Alternative positions for the wafer ID reader 24 will be apparent to those of skill in the art in light of the present disclosure. The wafer ID reader 24 identifies each unique silicon wafer 16, and transfers the information to a computer 32.")

(see column 4 lines 37-39, "The wafer ID reader 24 informs the computer 32 as to the identity of the silicon wafer 16 to be imaged for processing and storage purposes.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the optical techniques taught by the Lepejian reference to include the wafer ID reader taught by the Schemmel et al. reference to provide information identifying each silicon wafer including its location.

One of ordinary skill in the art would have been motivated to modify the optical techniques to include the wafer ID reader so that the processing system is provided with information identifying each silicon wafer including its location to facilitate accurate inspections of silicon dies on silicon wafers.

As per claim 29, the Lepejian reference discloses further comprising a sorting sub-station ("in-line defect inspection stations 12, 14, 16, 18") for using said database ("database 26") to automatically sort said plurality of die ("defects") into various physical bins (see column 11 lines 6-7, "die is rejected").

10. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,154,714 to Lepejian in view of USPN 5,943,551 to Schemmel et al. as applied to

claims 2, 3, 5, 16-26, 28 and 29 above, and further in view of USPN 6,129,278 to Wang et al.

As per claim 27, neither the Lepejian reference nor the Schemmel et al. reference discloses said die-strip code is a 2 dimensional matrix code that is placed on a surface of said die-strip.

The Wang et al. reference discloses

(see column 1 lines 12-16, "... bar codes (one-dimensional, such as UPC, Code 39, Code 128; two-dimensional, such as PDF 417, Code 49, Code 16K; etc.), matrix codes (Data Code, Code 1, Vericode, MaxiCode, etc.) and graphic codes (Glyph, etc.) ...")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the optical techniques taught by the Lepejian reference to include the silicon wafer ID reader taught by the Schemmel et al. reference to read various bar codes taught by the Wang et al. reference depending on the needs of the manufacturing facility.

One of ordinary skill in the art would have been motivated to further modify the optical techniques to include the silicon wafer ID reader to read various bar

codes to provide flexible optical techniques for use in diverse application of bar cades depending on the needs of the manufacturing facility.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to integrated circuit production/semiconductor fabrication in general:

USPN 6,875,640 B1 to Farnworth et al.

USPN 6,367,042 B1 to Phan et al.

USPN 6,337,221 B1 to Kim et al.

USPN 6,096,093 to Caywood et al.

USPN 4,928,002 to Corley et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 571.272.3679. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571.272.3687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Crystal J Barnes

CJB
13 June 2005